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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,656	02/09/2004	Yoshihisa Yamashita	10873.1397US01	1445
7590 11/20/2007 Hamre, Schumann, Mueller & Larson, P.C. P.O. Box 2902-0902 Minneapolis, MN 55402			EXAMINER DINH, TUAN T	
			ART UNIT 2841	PAPER NUMBER
			MAIL DATE 11/20/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/775,656

Applicant(s)

YAMASHITA ET AL.

Examiner

Tuan T. Dinh

Art Unit

2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 31 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,3-13 and 15-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-13 and 15-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☒ Other: See Continuation Sheet.

Continuation of Attachment(s) 6). Other: See attachment noted in form 892.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being obvious over Nakatani et al. (U.S. Patent 6,734,542).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As to claims 1, 3-13, 15-17, Nakatani et al. discloses an electronic component built-in module as show in figures 1-7 comprising:

a pair of opposed circuit substrates (405, see figure 4), each of which a wiring pattern (407) is formed an insulating base material containing a resin (405);  
an insulating layer (402) that is placed between the pair of circuit substrates and contains an inorganic filler and a resin composition containing a thermosetting resin;  
at least one electronic component (401) that is embedded and housed in the insulating layer (402) and mounted on the circuit substrate (405) (claim 15); and an

inner via (403) that is provided in the insulating layer (402) so as to make an electrical connection between wiring patterns (407) provided on different circuit substrates (405)

Nakatani does specific disclose in Tables 1-3 a glass transition temperature  $Tg_1$  of the resin composition contained in the insulating layer (402) and a glass transition temperature  $Tg_2$  of the resin of the insulating base material (405) included in each of the circuit substrates satisfy a relationship  $Tg_1 > Tg_2$ , and a difference between the glass transition temperature  $Tg_1$  and the glass transition temperature  $Tg_2$  is at least  $10^{\circ}\text{C}$ .

As to claim 3, Nakatani et al. discloses a plurality of the insulating layers that are provided.

As to claim 4, Nakatani et al. discloses the insulating layer (402) containing the inorganic filler in an amount of not less than 70% by weight and not more than 95% by weight.

As to claim 5, Nakatani et al. discloses the inorganic filler contains at least one selected from the group consisting of:  $\text{Al}_2\text{O}_3$ ,  $\text{MgO}$ ,  $\text{BN}$ ,  $\text{SiO}_2$ ,  $\text{SiC}$ ,  $\text{Si}_3\text{N}_4$ , and  $\text{AlN}$ , see column 12, lines 6-7.

As to claim 6, Nakatani et al. discloses the thermosetting resin containing at least one selected from the group consisting of: an epoxy resin, a phenol resin, and an isocyanate resin.

As to claim 7, Nakatani et al. discloses the at least one electronic component (401) comprises a semiconductor bare-chip.

As to claim 8, Nakatani discloses the inner via (403; 406) is formed from a conductive resin composition.

As to claim 17, Nakatani discloses the module wherein no electric component formed in the circuit substrates (405).

As to claims 9-13, Nakatani discloses all of the limitations of method of manufacturing an electronic component built-in module as shown in figures 1-6, and claims 1-8, and 15-17 do disclose all of the limitations of the final product of claimed language.

### ***Response to Arguments***

3. Applicant's arguments filed 08/31/07 have been fully considered but they are not persuasive.

Applicant argues:

Nakatani does not specific disclose  $Tg_1 > Tg_2$  and the different has at least  $10^0C$ .

Examiner disagrees. Nakatani disclose a layer (405) containing a resin, a layer (402) containing an inorganic filler and thermosetting resin, and with the fact that defines the resin having a Tg would be in a larger range (for example, a polyimide has Tg is about 250 degrees) and the inorganic filler with the thermosetting resin having a Tg in a range of maximum of 150 degrees. Thus, the Tg of resin is greater than the Tg of the inorganic filler with thermosetting resin (or greater than at least 10 degrees).

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gutierrez F. Diego can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Tuan Dinh  
November 10, 2007.

  
TUAN T. DINH  
PRIMARY EXAMINER

11/10/07